CLAIMS:

1. A latch circuit including:-

   a first latch portion including a first clock transistor; and

   a second latch portion including a second clock transistor;

   wherein the first and second clock transistors form a transistor clock pair and the first clock transistor has a different property or characteristic to the second clock transistor such that the 'hold period/follow period' ratio of the transistor clock pair is greater than 1.

2. A latch circuit according to claim 1, wherein the different property or characteristic comprises a difference in emitter area.

3. A latch circuit according to claim 2, wherein the emitter area of the first clock transistor is greater than that of the second clock transistor.

4. A latch circuit according to claim 3, wherein the emitter area of the first clock transistor is double that of the second clock transistor.

5. A prescaler circuit including a first and second latch circuit according to any one of the preceding claims.